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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,091	06/28/2002	Gilbert Wolrich	10559-310US1	7309

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,091	WOLRICH ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/27/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02/27/02, 06/09/04, 12/07/04, 12/13/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-22 are presented for examination.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1, 21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

3. As to claim 1, The language of the claim raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. For example, the relatively addressable window od registers are not directed to statutory subject matter because no functional material ahs been found into the claim. When nonfunctional descriptive material is recorded on some computer-readable medium, it is not statutory since no requisite functionality is present to satisfy the practical application requirement. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make it statutory. Such a result would exalt form over substance. In re Sarkar, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 1978) ("[E]ach invention must be evaluated as claimed; yet semantogenic considerations preclude a determination based solely on words appearing in the claims. In the final analysis under 101, the claimed invention, as a whole, must be evaluated for

what it is.") (quoted with approval in Abele, 684 F.2d at 907, 214 USPQ at 687). See also In re Johnson, 589 F.2d 1070, 1077, 200 USPQ 199, 206 (CCPA 1978) ("form of the claim is often an exercise in drafting"). Thus, nonstatutory music is not a computer component and it does not become statutory by merely recording it on a compact disk. Protection for this type of work is provided under the copyright law. IN instant case, the windows of registers are not found to have stored data of any type, therefore, no functional material can be fond in the claim. As to the language of "executing thread" , in view of applicant's teaching (see page 2, lines 13-15), applicant's invention includes freeware from the internet, and internet is not tangible. Therefore, It is directed to non-statutory subject matter. As to the preamble reciting the "maintaining execution threads in parallel multithreaded processor", no details of maintain the thread execution in a parallel multithreaded processor can be found in the body of the claim. "Maintain execution thread" is not the same as execute the thread, and since applicant already taught (page 2, lines 13-15) the use of freeware over the internet, the maintain of the execution threads in parallel multithreaded processor is read as maintain the thread over the internet, which is not necessary implemented into the hardware , and therefore, non-tangible (e.g. the internet medium etc).

4. As to claim 21, Claim 21 is not limited to tangible embodiments. In view of Applicant's disclosure, specification page [2], line [3-15], the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., [hardware based processor]) and intangible embodiments (e.g., [internet]). As

such, the claim is not limited to statutory subject matter and is therefore non-statutory.

the internet medium is not tangible, therefore, it is non-statutory.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 and clams 12, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 18, 2, respectively, of copending Application No. 09/760,509. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons given below.

6. As to claim 1, although copending claim 18 (claim 18 included limitations of claims 15 and claim 17) did not recite the "parallel" multithreaded processor as clamed in the current claim1, the copending claim 18 recites executing multiple context threads and reading and writing of the dual port memory at the same cycle (see parent claim 15), it would have been obvious to one of ordinary skill the art to use parallel threaded execution because one of ordinary skill in the art should be able to recognize the need

for including a parallel processor in the multiple threaded execution in order meet the demand of reading and writing at the same cycle, and therefore, to increasing the processing bandwidth at a given time, and in doing so, provided motivation.

7. As to claim 12, although claim 2 (claim 2 included limitations of claim 1) did not specifically recite the arbitration access to the microengine as recited in the current claim 12, it would have been obvious to one of ordinary skill in the art to use arbitration to a microengine because the copending claim 2 also taught an arithmetic execution unit to process data for execut8ingthe multiple context threads, which would have been recognizable by one of ordinary skill in the art that the arbitration was also applicable into the multiple thread execution for the access by the multiple threads at a given cycle, thereby providing a predefined sequence of the multiple threaded executions, and in doing so , provided a motivation.

8. As to claim 21, although copending claim 2 did not recite the computer program product readable on a computer readable medium as clamed in claim 21, the copending claim 2 also taught a two ported random access memory, therefore, one of ordinary skill in the art should be able to recognize the random access memory could be used for storing a computer program product in order to perform a predetermined process because the random access memory was also a computer readable medium.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (The Compiler for Supporting Multithreading in Cyclic Register Windows", 1996.

10. As to claim 1, Cheng disclosed a method of maintaining execution threads in a parallel multithreaded processor()see page 57 , the multithreaded mechanism and the sparc processor) comprising at least :

a) accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows (see of divided registers in windows and the window pointer (CWP) for the relative addressable windows, see also In and Local registers in a register window in page 58, see also the Thread procedures)

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

11. Claim 1-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Panwar et al. (5,870,597).

12. As to clam 1, Panwar disclosed maintaining execution thread in a parallel multithreaded processor (see consistent implementation of multithreaded processor 102 in col.6, lines 40-44) comprising accessing, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows of registers that are relatively addressable per thread (see the registers sets organized into register windows in col.2, lines 40-65, see the window pointer CWP for the relative addressable registers, see also the movable windows within the register file in col.7, lines 40-67, col.8, lines 1-5).

13. As to claim 2, Panwar also included same relative register address (window pointer) but access different banks od registers (register sets, see col.2, lines 40-65).

14. As to claim 3, Panwar's elative address also divided the register banks (register sets) into windows across address width of general purpose registers (see the general purpose registers in col.2, lines 40-65).

15. As to claim 4, Panwar also accessed any of the windows with a starting point (see the manipulation of the window position and the window permitted the movable subsets of registers in col.2, lines 40-65, see also the logical and index address in col.2, lines 67-68, col.3, lines 1-6).

16. As to claim 5, Panwar also organized the register sets in to windows according to the number of threads (see the 3 register windows per one instruction bundle in fig.5, col.9, lines 5-33, see also multithreaded in col.2, lines 40-65).

17. As to claim 6, Panwar also allowed different windows perform different functions (see different processes call their own windows in col.7, lines 39-46).

18. As to claim 7, Panwar also taught dual port memory (see the multiported memory in col.1, lines 44-45).

19. As to claim 8, Panwar also allowed any starting point (see the manipulation of the window position and the window permitted the movable subsets of registers in col.2, lines 40-65, see also the logical address in col.2, lines 67-68, col.3, lines 1-6).

20. As to claim 9, Panwar also included absolute address (see the physical addresses in col.2, lines 53-65).

21. As to claim 10, Panwar also included source field and destination field (see destination and source in col.2, lines 66-67, col.6, lines 1-5).

22. As to claim 11, see offset in col.7, lines 54-56).

23. As to claim 12 , Panwar taught at least a hardware based multi-threaded processor (see the consistent use of multithreaded processor in col.6, lines 40-44) comprising:

a) control logic [204] [206] including context event switching logic, the context switching logic arbitrating access to a microengine for a plurality of executable threads (see the functions performed by scheduling units 204 and 206 in col.6, lines 27-58, see also the Save and Restore of the registers in col.7, lines 62-67, col.8, lines 1-41);

b) an arithmetic logic unit to process data for executing threads (see either 208 integer or 210 floating point , col.6, lines 31-33); and

c) a register set that is organized into a plurality of relatively addressable windows of registers that are relatively addressable executable thread (see col.7, lines 40-46).

24. As to claim13, Panwar also included :

an instruction decoder (see instruction decode in col.6, lines 63-64, col.7, lines 11-13); and program counter units to track executing threads (see the redirection of execution of multiple treaded operations by the dispatch unit 206 in col.6, lines 27-44, see also instruction identified by controller 502 in col.9, lines 54-60, see also a branch identifier in col.11, lines 29-33).

25. As to claim 14, Panwar also included program counters units are maintained in hardware (see the dispatcher 206 and controller 502).

26. As to claim 15, Panwar also taught register banks (sets) organized into windows across an address width of the general purpose register set with each window relatively accessible by a corresponding thread (see general purpose registers in col.2, lines 39-65, see the register windows movable by a process or program in col.7, lines 40-47, see the logical and index addresses in col.2, lines 62-67, col.3, lines 1-5 for relative addresses).

27. As to claim 16, Panwar also taught relative addressing allows access to any of the registers relative to the starting point of a window of registers (see the manipulation of the window position and the window permitted the movable subsets of registers in col.2, lines 40-65, see also the logical address in col.2, lines 67-68, col.3, lines 1-6). .

28. As to claim 17, Panwar also taught number of windows of the register set is according to the number of threads that execute in the processor (see the 3 register windows per one instruction bundle in fig.5, col.9, lines 5-33, see also multithreaded in col.2, lines 40-65).

29. As to claim 18, Panwar also taught relative addressing allow the multiple threads to use the same control store and locations while allowing access to different windows of register and perform different functions (see different processes with their own windows in col.7, lines 39-47).

30. As to claim 19, Panwar also taught dual ported memory (see col.1, lines 44-45).

31. As to claim 20, Panwar also taught a micropropnmmed processor unit (see program running on microprocessor in col.2, lines 30-41).

32. As to claim 21, Panwar taught a computer program product residing on a computer readable medium (see fig.1, col.5, lines 120) for managing execution of multiple threads (see multiple treaded operation in col.6, lines 36-44) in a multithreaded processor comprising instructions causing a processor to: access, by an executing thread in the multithreaded processor, a register set organized into a plurality of relatively addressable windows of registers that are relatively addressable per

thread (see movable register windows col.2, lines 40-65, coll7, lines 40-46, see also the window pointers).

33. As to claim 21, Panwar also included absolutely addressable registers where any one of the absolutely addressable registers may be accessed by any of the threads by providing the exact address of the register (see the physical address of the registers in col.9, lines 50-53).

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a)Shaylor (6,408,325) is cited for the teaching of the register sets in windows with the context switching technique (see col.3, lines 1-17, col.4, lines 29-51, see col.5, lines 32-43).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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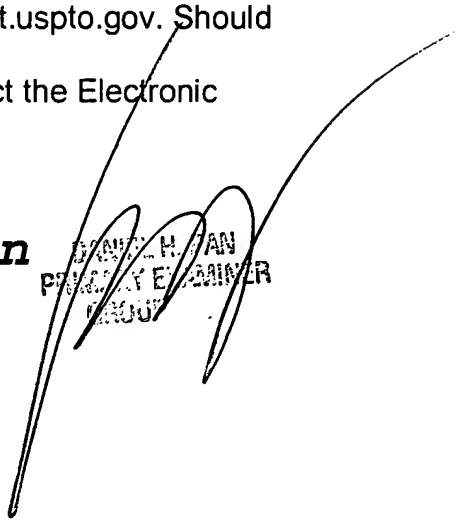

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